Analog Devices
Software Defined Radio

AD9361 / AD9364
Offering & Support Model

June 9th, 2014
Agenda

- History
- AD9361 / AD9364
  - Product
- Target Segments and Applications
- Support Model
  - Online Customer Support model
- Live AD9361 Demo
- Q&A
What Is a Software Defined Radio?

- A software defined radio system (SDR) is a radio communication system where components that have been typically implemented in hardware (e.g., mixers, filters, amplifiers, modulators/demodulators, detectors) are instead implemented by means of software on a personal computer or embedded system.
- While the concept of SDR is not new (circa ~1970 DoD labs), many techniques which used to be only theoretically possible are now being implemented due to the rapidly evolving capabilities of analog and digital electronics.

Why SDR?

- Makes RF hardware easier
- Easy to add new features, since they are all in software
- Easier to have one set of hardware handle multiple modulation techniques
Traditional RF Evaluation Platforms (Antenna to Bits, circa 2010)

- Discrete single product evaluation boards, connected with wires
  - 6 power supplies
  - 4 different USB applications
- Not easy to replicate, or use as part of a SDR prototyping solution
- Needed small form factor, open design
Direct Conversion Technique (FMComms1)

- AD9122 16-Bit 1250MSPS Modulator
- ADL5375 Frequency Synthesizer
- ADL5602 20dB Fixed Gain
- ADL5380
- AD8366
- AD9643
- AD9548
- AD9523-1
- ADF4351
- ADL5605/6
- AD9122 DAC runs at 1000MSPS, due to max speed of AD9523-1

- LPC (32 Data + 3 CLK LVDS) FMC Connector (500MHz)
- 1W Amp
- Power
- 5V @ 500mA
- Optional Front End
- 400MHz to 4000MHz Low Noise Amplifier Tuned for Frequency
- Non-SMA connector
- SMA connector
- Solder bump jumper
- Pi network
- SPI

- ADL5523
- 400MHz to 4000MHz
- Transmission power control is accomplished by adjusting baseband data
- Optional Front End
- RF output power control is accomplished by adjusting baseband data
FMCOMMS1 Board – Tx, Rx, Clocks, Power circa ~2012

- **AD9548**: Network Clock Generator/Synchronizer
- **AD9643**: ADC 14-bit, 250 MSPS
- **ADG3304**: 4 Channel, Bidirectional, Logic Level Translator
- **AD8366**: 0.25dB Step Size VGA, 600MHz Bandwidth
- **ADL5380**: Demodulator 400 – 6000MHz
- **ADL5375**: Modulator 400 MHz to 6000MHz
- **AD9122**: DAC, 16-Bit, 1250 MSPS
- **ADF4351**: Rx Synthesizer 35 MHz to 4400 MHz
- **ADF4351**: Tx Synthesizer 35 MHz to 4400 MHz

**Notes:**
- AD9122 DAC runs at 1000MSPS, due to max speed of AD9523-1
Software Defined Radio Customer Needs
Pent up demand for a much better integrated SW-defined RF TRx

- SDRs becoming OEM necessity across many apps/markets
  - Enable one common reprogrammable radio platform for multiple radio schemes
  - Offer flexibility and configurability, field upgradable
- Today’s available integrated wideband agile TRx solutions have limited performance, limited tunable bandwidths
  - Unacceptable for many applications
- Many OEMs lack the capability or resources to implement practical and cost-effective SDRs
  - HW & RF signal chain design expertise, SW development
  - Time-to-market delays, costs to design discrete SDRs

Need for a complete, integrated RF TRx solution with a reference design that includes production-ready software and drivers
FMCOMMS2 – Moore’s Law in action - Now

**AD9361**
RF Agile Transceiver™
70 MHz – 6000 MHz Turning range
200kHz – 56 MHz RF channel Bandwidth

**ADP1755**
Low V\textsubscript{in} / V\textsubscript{out} LDO

**ADP2164**
synchronous, step-down dc-to-dc regulator

**M24C02**
EEPROM

**40 MHz**
Crystal

**AD7291**
8-channel, SAR ADC
Housekeeping
AD9361 / AD9364 Under the Hood

- **AD9361**: 2 Rx + 2 Tx
- **AD9364**: 1 Rx + 1 Tx
- **Major sections:**
  - RF input/output paths
  - RF PLL/LO
  - Clock generation
  - ADC/DAC
  - Digital filters
  - Digital interface
  - Enable state machine
  - RX Gain (AGC)
  - TX Attenuation
  - Aux DAC/ADC and GPOs
  - Analog and Digital Correction/Calibration
RF PLL and LO Generation

70MHz to 6GHz operation covers FM radio, ISM Bands, TV whitespace, 2G/3G/3G cellular, WiFi bands…. and everything in between!
Complexity of Next Generation SDR Systems

- RF Design Skills
- Digital Hardware
- SOC System Assembly
- DSP Hardware
- Software Development

Requires 5 different design skills to be successful. ADI references show working example!
Rapid Proto-typing with AD-FMCOMMS[234]-EBZ

**Hardware**
- **AD-FMCOMMS2-EBZ (AD9361)**
  - Narrow RF Tuning Range
- **AD-FMCOMMS3-EBZ (AD9361)**
  - Wide RF Tuning Range
- **AD-FMCOMMS4-EBZ (AD9364)**
- **Works with:**
  - Xilinx Zynq based solutions, including ZC706 (shown), ZC702, and Zedboard
  - Xilinx Kintex (KC705) and Virtex (VC707)

**Software**
- **Device drivers**
  - Linux and/or No-OS
- **FPGA HDL**
- **IIO scope**
  - Data visualization application
  - Graphical configuration application
Applications for the AD9361/AD9364 SW-Defined RF Transceiver IC

- Defense electronics
  - Radar, handheld and manpack battlefield radios
- RF test equipment and instrumentation
- Communications and telemetry equipment
- Communications infrastructure
  - Femtocell / picocell / microcell basestations, data card dongles
- General software-defined radio platforms
Applications Example 2 x 2 MIMO

Single AD9361 Transceiver covers all LTE channel bandwidths

Attach opportunities:
ADP5050/51/52/53 power solution
Linear Amplifiers e.g. ADL5601/2/4, ADL5320
LNAs in some applications: ADL5521/ADL5523
Tools to help you design with the AD9361/AD9364

- **Hardware package:**
  - Schematics, Layout, Datasheet

- **Software:**
  - Complete Linux and no-OS drivers

- **HDL**
  - Generic Verilog, verified on Xilinx

- **Design Tools**
  - FIR Filter designer (MATLAB)
  - System level simulation (MATLAB/Simulink)
Design Files on www.analog.com/ad9361rftransceiver

Download the complete design file resource package.
The AD9361 is a high performance, highly integrated RF Agile Transceiver™. Its programmability and wideband capability make it ideal for a broad range of transceiver applications. The device combines an RF front end with a flexible mixed-signal baseband section and integrated frequency synthesizers, simplifying design-in by providing a configurable digital interface to a processor. The AD9361...
AD-FMCOMMS[234]-EBZ doc on Wiki

http://wiki.analog.com/resources/eval/user-guides/ad-fmcomms2-ebz
http://wiki.analog.com/resources/eval/user-guides/ad-fmcomms3-ebz
http://wiki.analog.com/resources/eval/user-guides/ad-fmcomms4-ebz

1. Introduction
2. Quick Start Guides
   I. Linux on ZC702, ZC706, ZED
3. Hardware (including schematics)
   I. Functional Overview & Specifications
   II. Characteristics & Performance
   III. Configuration options
4. Reference HDL Design
   I. Digital Interface Timing Validation
5. Software
   I. Linux
      a. ZC702, ZC706, ZED
      b. Applications
         α. Command Line/Shell scripts
         β. IIO Scope
   II. No-OS drivers
6. Production Testing Process
7. Additional Documentation about SDR Signal Chains
   I. The math behind the RF
8. Help and Support
Device Drivers on Wiki

- **Linux**
  - Released under GPL license
  - High Level API
  - Easy interface to various high level programming languages: C++, Python, Shell, etc.

- **No-OS**
  - Released under BSD type license
  - No-OS device drivers are purely written in C and feature an Hardware abstraction layer (HAL)
  - Similar feature set as Linux device driver

```c
int main(){
    phy = ad9361_init(&defLTE20);
ad9361_set_rx_lo_freq(phy, 2400000);
}
```
Device Driver Documentation/Description

- Doxygen files for no-os code
  - [http://analogdevicesinc.github.io/ad9361](http://analogdevicesinc.github.io/ad9361)

[Image of Doxygen files and AD9361 data structures]
IIO: A New(er) Kernel Subsystem for Converters

- The Linux Industrial I/O (IIO) subsystem is intended to provide support for devices that, in some sense, are analog-to-digital or digital-to-analog converters
  - Devices that fall into this category are:
    - ADCs
    - DACs
    - Accelerometers, gyros, IMUs
    - Capacitance-to-Digital converters (CDCs)
    - Pressure, temperature, and light sensors, etc.
    - RF Transceivers (like the AD9361/AD9364)
  - Can be used on ADCs ranging from a 1MSPS SoC ADC to >250 MSPS industrial ADCs
  - Developed during 2009, committed Jan 2010, moved out of staging Nov 2011, now in all mainline Linux kernels.
IIO Scope for Real Time Data Visualization

- Runs directly on Xilinx Zynq
  - HDMI monitor, USB Keyboard/Mouse
- Visualize data:
  - Frequency
    - simple and complex FFT
  - Time Domain
  - Constellation (I vs Q)
- Capture data:
  - Save sequences to file
  - Supports different formats
- Drive data:
  - Dual tone polyphase DDS
  - Arbitrary Waveforms and Sample files
IIO Scope: Understands AD9361 / AD9364

- **Configure and Control**
  - Rx/Tx LO frequency
  - TRX control
  - Rx/Tx Sampling Rates
  - RF Bandwidths analog and digital filters
  - Gain and AGC modes
  - Quadrature and DC tracking control

- **Monitor**
  - Gain
  - RSSI
  - Etc.
IIO Server/Client

- **ADI IIO Command Server**
  - Runs on and embedded target under Linux
  - Manages real-time data exchange over TCP or UDP between the target and a remote client
  - Data Exchange is based on a simple communication protocol

- **Matlab IIO Client**
  - Implements the communication protocol with the IIO Server
  - Based on the UDPReceiver / UDPSender classes from the Mathworks DSP toolbox
  - Controls the embedded target using specific commands
  - Acquires real-time data from the embedded target

- **C Client**
  - Generic C source

- **C# Client**
  - C# source

- **Visual Analog Client**
  - Visual Analog
Community Support On EngineerZone

◆ Three Very Active Communities
  ● FPGA Reference Designs
    ◆ 363+ discussions
  ● Linux and No-OS Drivers
    ◆ 123+ discussions
  ● Wide Band RF Transceivers
    ◆ 25+ discussions in 2 months

◆ Support a variety of questions
  ● AD9361 and AD9364 on Wide Band RF Transceivers Community
  ● FPGA on FPGA Reference Designs Community
  ● Software on Linux Drivers Community
AD9361 / AD9364 Support Model

- Buy AD-FMCOMMS2-EBZ for RF evaluation
  - AD9361 with narrow RF tuning range (optimized for 2.4GHz)
- Buy AD-FMCOMMS3-EBZ for rapid prototype
  - AD9361 with wide RF tuning range (70 MHz - 6GHz)
- Buy AD-FMCOMMS4-EBZ for either
  - AD9364 with narrow (2.4GHz) and wide ranges (70MHz - 6GHz)
- AD9361 Design Files

- Application and Drivers for Linux and No-OS
  - Linux IIO: Linux Abstraction for Data Converters
- HDL
- PCB Schematics, Gerbers, BOM

- Online support via EngineerZone
  - Wideband RF Transceiver Community
  - FPGA Reference Design Community
  - Linux and Microcontroller Devices Drivers Comm.

analog.com
wiki.analog.com
ez.analog.com
Demo Overview

- Xilinx Zedboard ($395)
  - HDMI monitor/capture card
  - USB Keyboard Mouse
- AD-FMCOMMS2-EBZ (AD9361) $750
- SD Card, with ADI image on it
  - Linux + IIO Scope
Demo: IIO Scope

- **AD9361 control**
  - Dual DDSes
  - Arbitrary data loads
  - Set Tx/Rx Frequencies

- **Visualization**
  - Time domain
  - Constellation
  - Frequency domain
AD9361 Key Facts & Features

- **2 x Tx, 2 x Rx Channels**
- Complete, highly configurable RF transceiver
- Tunable RF bandwidth 70 MHz to 6.0 GHz
- Programmable channel bandwidth; 200 kHz to 56 MHz
- Integrated 12-bit ADCs and DACs, LNAs, mixers, analog filters, clocking solution, frequency synthesizers
- Superior receiver sensitivity with noise figure <2.5 dB
- Highly-linear broadband transmitter with EVM: ≤ -40 dB
- Integrated low phase noise fractional-N synthesizers
- 128 complex-tap programmable FIR filters
- Meets 3G/4G wireless standards
- Ideal for Software Defined Radio

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<th>RF Bandwidth</th>
<th>Channel Bandwidth</th>
<th>Rx Noise Figure</th>
<th>Tx EVM</th>
<th>Tx Noise</th>
<th>Package</th>
<th>Temp</th>
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<td>70MHz to 6GHz</td>
<td>200kHz to 56MHz</td>
<td>2.5dB</td>
<td>&lt;40dB</td>
<td>&lt;155dBm/Hz</td>
<td>10mm x 10mm CSPBGA</td>
<td>-40°C to +85°C</td>
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AD9364 Key Facts & Features

- **1 x Tx, 1 x Rx Channels**
- Complete, highly configurable RF transceiver
- Tunable RF bandwidth 70 MHz to 6.0 GHz
- Programmable channel bandwidth; 200 kHz to 56 MHz
- Integrated 12-bit ADCs and DACs, LNAs, mixers, analog filters, clocking solution, frequency synthesizers
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Summary

- **Sampling and Orderable!**
  
<table>
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<tr>
<th>Part Number</th>
<th>Description</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD9361</td>
<td>1ku: US$175</td>
<td></td>
</tr>
<tr>
<td>AD9364</td>
<td>1ku: US$130</td>
<td></td>
</tr>
<tr>
<td>AD-FMCOMMS2-EBZ</td>
<td></td>
<td>$750</td>
</tr>
<tr>
<td>AD-FMCOMMS3-EBZ</td>
<td></td>
<td>$750</td>
</tr>
<tr>
<td>AD-FMCOMMS4-EBZ</td>
<td></td>
<td>$399</td>
</tr>
<tr>
<td>AES-ZSDR2-ADI-G</td>
<td>SDR evaluation kit for AD9361 (from Avnet)</td>
<td>$1495</td>
</tr>
<tr>
<td>AES-ZSDR3-ADI-G</td>
<td>SDR development kit for AD9361 (from Avnet)</td>
<td>$3595</td>
</tr>
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- **Target segments**: Aerospace & Defense, CIFR, Electronic Test & Measurement

- **Comprehensive Online Customer Support for all AD9361/AD9364 reference boards and software**
  
  - FPGA Reference Designs Community
  - Wide Band RF Transceiver Community
A direct-conversion transceiver, also known as homodyne, synchrodyne, or zero-IF transceiver, is a radio transceiver design that (de)modulates the radio signal using a local oscillator (LO) whose frequency is identical to, or very close to, the carrier frequency of the intended signal.

- Carrier frequency = local oscillator (LO) frequency
- Attractive due to simplicity of the signal path
- Suitable for high levels of integration
- Allows wider bandwidth designs
Homodyne Transmitter Advantages and Challenges

**Advantages:**
- Low component count leads to lower system cost and power consumption
- Direct up-conversion produces less mixing product spurs
- Requires fewer filters

**Challenges:**
- During the analog modulation process, gain and phase mismatches of IQ signals have a direct impact on sideband suppression performance
- Out of band transmissions
  - LO / carrier leakage
  - I/Q mismatch causes image in the output spectrum
    - This results in degraded error vector magnitude (EVM) at the receiver, which in turn degrades the bit error rate (BER)
Homodyne Receiver Advantages and Challenges

**Advantages:**
- Low component count leads to lower system cost
- No image reject filter needed
- Filtering requirements more relaxed at baseband
- Gain stages at baseband provide power savings

**Challenges:**
- DC offset appearing at baseband
  - Self mixing
  - Offset voltages
- Images appearing symmetrically about zero frequency
  - I/Q mismatches in phase and amplitude
- Even order nonlinearities
  - Two high frequency interferers close to the channel of interest can result in even order nonlinearities that fall within the band of interest
Back to Basics: Euler’s Formulas

\[ \cos \omega_0 t = \frac{A}{2} (e^{j\omega_0 t} + e^{-j\omega_0 t}) \]

\[ \sin \omega_0 t = \frac{A}{2j} (e^{j\omega_0 t} - e^{-j\omega_0 t}) \]

- \( \sin \omega_0 t \) is 90° out of phase with respect to \( \cos \omega_0 t \)
- With perfect amplitude and phase matching the signal content at \(-\omega_0\) cancels
Amplitude and Phase Mismatch

**Amplitude Mismatch**

\[
x(t) = A \cos \omega_0 t + jB \sin \omega_0 t \]

\[
x(t) = \frac{A}{2} (e^{j\omega_0 t} + e^{-j\omega_0 t}) + \frac{B}{2} (e^{j\omega_0 t} - e^{-j\omega_0 t})
\]

\[
x(t) = \frac{A}{2} e^{j\omega_0 t} + \frac{A}{2} e^{-j\omega_0 t} + \frac{B}{2} e^{j\omega_0 t} - \frac{B}{2} e^{-j\omega_0 t}
\]

\[
x(t) = \frac{A + B}{2} e^{j\omega_0 t} + \frac{A - B}{2} e^{-j\omega_0 t}
\]

**Phase Mismatch**

\[
x(t) = \cos(\omega_0 t + \theta) + j \sin \omega_0 t
\]

\[
x(t) = \frac{1}{2} e^{j\omega_0 t} e^{j\theta} + \frac{1}{2} e^{-j\omega_0 t} e^{-j\theta} + \frac{1}{2} e^{j\omega_0 t} - \frac{1}{2} e^{-j\omega_0 t}
\]

\[
x(t) = \frac{1}{2} (e^{j\theta} + 1) e^{j\omega_0 t} + \frac{1}{2} (e^{-j\theta} - 1) e^{-j\omega_0 t}
\]

Desired Signal

Image

\[
\]
Noise and Imperfections in transmit and receive signal chains result in demodulated voltages which are displaced from their ideal location.

Error Vector Magnitude expresses this dislocation

Large EVM will result in Symbol Errors and degraded Bit Error Rate

Higher Order Modulation Schemes → Symbols Closer Together → EVM More Critical
Effects of Gain, Offset, and Phase Errors

- Gain Error
- Offset Error
- Phase Error
What Is Causing the Poor Quality of This Demodulated Constellation?

- Very poor LO Quadrature Phase Split (in DMOD)
- DC Offset of the complete constellation (probably LO to RF leakage in Tx)
- Noise has enlarged the footprint of the constellation points (poor Receiver Noise Figure)

Symbol Decision Threshold
If the symbol lands on the edge or outside of the box, bit errors will occur.
Effects of I/Q Mismatch

** Images Occupy BW **

** Interfere with Desired Signal **

Desired Signal

Gain Error

Phase Error

** EVM Degradation **